REPORT R-367 SEPT. 1967

CSL COORDINATED SCIENCE LABORATORY

AN IMPROVED POLARITY COINCIDENCE DETECTOR

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This work was supported by the Joint Services Electronics Program (U. S. Army, U. S. Navy, U. S. Air Force) under Contract DA 28 043 AMC 00073(E)

An Improved Polarity Coincidence Detector

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Abstract

A Polarity Coincidence Detector has been constructed with increased sensitivity and sufficient threshold stability to allow integration times in excess of 10^6 sec. The system uses sampling at four phase locations, thereby increasing the signal count and shortening the integration time for a given accuracy by eliminating the necessity for measuring the noise separately. The modulation frequency can be varied between 50 Hz and 50 kHz without adjusting the location of the sampling pulses. Solid state circuitry is used throughout the system. The straight counters are replaced by arithmetic units, resulting in greater dependability.

In this report we describe the theory, design, and performance of an improved polarity coincidence detector which, compared to the previously described system[1], offers the advantages of increased sensitivity, greater stability, and more convenient operation.

I. Theory

The Polarity Coincidence Principle

For the sake of self-consistency we review briefly the major features of the polarity coincidence scheme; for details the reader is referred to reference 1.

In the PCD scheme, the waveform, consisting of a signal of known frequency but unknown phase embedded in noise, is sampled with pulses at the signal frequency and coincidences are recorded whenever the waveform and the sampling pulse have the same polarity. If the signal has the form $A(t) = \sqrt{2}\ U \sin(\omega t+\phi)$ and we assume narrow band gaussian noise, the fraction of sampling pulses in phase at 0^o resulting in a coincidence is given by

$$\frac{n(0^o)}{n_o} = \tfrac{1}{2}\left[1 - \operatorname{erf}\left(\frac{x_o}{\sigma\sqrt{2}} - \frac{U}{\sigma}\cos\phi\right)\right] \qquad (1)$$

where σ^2 is the variance of the noise and x_o the theoretical amplitude which the wave must equal for a coincidence to be registered. Similarly for a sampling phase of 90^o we have

$$\frac{n(90^o)}{n_o} = \tfrac{1}{2}\left[1 - \operatorname{erf}\left(\frac{x'_o}{\sigma\sqrt{2}} - \frac{U}{\sigma}\sin\phi\right)\right] \qquad (2)$$

The unknown thresholds can be determined by measuring the noise without signal. Elimination of the signal phase ϕ yields for small values of u/σ

$$\frac{U}{\sigma} = \frac{\pi^{\frac{1}{2}}}{n_o}\left[\left(n(0^o) - n_N(0^o)\right)^2 + \left(n(90^o) - n_N(90^o)\right)^2\right]^{1/2} \qquad (3)$$

where n_N are the counts of the noise alone.

The relative error of the counts is given by

$$\left(\frac{\Delta n}{n}\right)^2 = \frac{1}{n}\left[1 + \frac{4}{\pi}\sum_{k=1}^{n-1} \arcsin \rho_N \left(\frac{2\pi k}{\omega}\right)\right] = \frac{\beta^2}{n} \qquad (4)$$

where ρ_N is the normalized correlation function of the noise, β is a function of the spectral density of the noise, it increases with decreasing bandwidth. If the spectral density of the noise extends up to the sampling frequency, β is very nearly unity.

This scheme can be refined in several respects, resulting in a greater sensitivity and in more convenient operation.

Improved PCD

The main deficiencies of the simple PCD-system are

a) The phase must be set for each frequency

b) The noise must be measured separately

c) The coincidence thresholds in the two channels are different

d) The available information about the signal has not been utilized fully.

A great improvement in the performance of the PCD can be achieved if the waveform is sampled 4 times per period (at 0^o, 90^o, 180^o, and 270^o) and if the coincidence thresholds are made equal in all channels. In this case we have for small signal to noise ratios

$$\left(\frac{n}{n_o}\right)_0 = \tfrac{1}{2} - \frac{1}{\sigma\sqrt{\pi}}\left(\frac{x}{\sqrt{2}} - U\cos\phi\right)$$

$$\left(\frac{n}{n_o}\right)_{90} = \tfrac{1}{2} - \frac{1}{\sigma\sqrt{\pi}}\left(\frac{x}{\sqrt{2}} - U\sin\phi\right)$$

$$\left(\frac{n}{n_o}\right)_{180} = \tfrac{1}{2} - \frac{1}{\sigma\sqrt{\pi}}\left(\frac{x}{\sqrt{2}} + U\cos\phi\right)$$

$$\left(\frac{n}{n_o}\right)_{270} = \tfrac{1}{2} - \frac{1}{\sigma\sqrt{\pi}}\left(\frac{x}{\sqrt{2}} + U\sin\phi\right) \qquad (5)$$

Combining these we obtain

$$\left(\frac{n}{n_o}\right)_0 - \left(\frac{n}{n_o}\right)_{180} = \frac{2}{\sigma\sqrt{\pi}}\,U\cos\phi$$

$$\left(\frac{n}{n_o}\right)_{90} - \left(\frac{n}{n_o}\right)_{270} = \frac{2}{\sigma\sqrt{\pi}}\,U\sin\phi \qquad (6)$$

We see that not only has the unknown threshold been eliminated but also the signal has increased by a factor of 2.

The output signal-to-noise ratio is thus given by

$$\left(\frac{S}{N}\right)_{out} = \frac{\left[(n_o - n_{180})^2 + (n_{90} - n_{270})^2\right]}{(\Delta n)^2} = \frac{4U^2}{\sigma^2\pi}\,\frac{n_o}{\beta^2} \qquad (7)$$

Since the input signal-to-noise ratio is given by $\left(\frac{S}{N}\right)_{in} = \frac{U^2}{\sigma^2}$, the ratio of output signal to noise to input signal to noise is written as

$$\frac{(S/N)_{out}}{(S/N)_{in}} = \frac{4n_o}{\pi\beta^2} \qquad (8)$$

For narrow band input noise with spread $\Delta\omega$, β^2 is given by $\frac{\omega_o}{\Delta\omega}$. n_o is the total number of reference cycles given by $f_o T = \frac{\omega_o T}{2\pi}$ where T is the integration time. We thus have

$$\frac{(S/N)_{out}}{(S/N)_{in}} = \frac{4\omega_o T\Delta\omega}{2\pi^2\omega_o} = \frac{2\Delta\omega T}{\pi^2} = R_{PCD} \tag{9}$$

It is of interest to compare the performance of this improved PCD device with an ideal synchronous detector. This may be represented by a multiplier which multiplies the input signal plus noise with the reference, followed by an ideal averaging filter. Assuming that the signal and reference are given by

$$S = U \sin \omega t$$

$$L = A \sin \omega t \tag{10}$$

and the noise is narrow band with the spectral density

$$S_N = \begin{cases} A_o; & fo - \frac{\Delta f}{2} < | f | < fo + \frac{\Delta f}{2} \\ 0; & \text{otherwise} \end{cases} \tag{11}$$

and the response function of the filter is given by

$$h(t) = \begin{cases} \frac{1}{T}; & o < t < T \\ 0; & \text{otherwise} \end{cases} \tag{12}$$

The output signal-to-noise ratio is given by

$$(S/N)_{out} = \frac{U^2}{2\pi\sigma^2}\Delta\omega T, \tag{13}$$

while the input ratio is

$$(S/N)_{in} = \frac{U^2}{2\sigma^2} . \tag{14}$$

Hence, the ratio of output to input signal-to-noise ratios becomes

$$\frac{(S/N)_{out}}{(S/N)_{in}} = \frac{\Delta\omega T}{\pi} = R_{SD} .$$

Thus, comparing with the PCD, we have

$$\frac{R_{PCD}}{R_{SD}} = \frac{2}{\pi},$$

which is slightly better than - 2 dB.

II. PCD Circuitry

Theory of Operation

The present model of the PCD determines the polarity of its input at four symmetric points during a modulation cycle. This is accomplished as follows. The input signal plus noise is sampled at four times the modulation frequency and then limited. The polarity of each sample is determined by a single coincidence circuit. The pulse resulting from a coincidence is then steered to the output corresponding to the phase of the sample. The pulses at the four outputs are then counted and processed to obtain the signal to noise ratio of the input.

Fig. 1 shows a simplified block diagram of the PCD. The sampling circuit consists of the linear amplifier $\alpha 1$, the sample-and hold circuit, the limiting amplifiers $\alpha 2$ and $\alpha 3$, the level shifter, LS, and the pulser P2. The input noise plus signal, pre-filtered to remove all harmonics of the modulation frequency, is amplified in $\alpha 1$ and applied to the sampler. When P2 is triggered, a pulse of approximately one-half microsecond duration activates the sampler. During this interval it acts as an amplifier of unity

gain, transmitting the instantaneous voltage at the input to the limiting amplifiers and the level shifter, where the limited voltage level is adjusted to the appropriate logic level. When the pulse from P2 disappears, the sampler output is held to the value set. Hence, the level at D is stored in preparation for polarity determination.

The polarity of the sample is determined by the pulser P3 and the coincidence circuit NA1. When P3 is triggered, the pulse thus formed is inverted and applied to NA1, along with the voltage at D, set previously. For D negative the pulse is transmitted through NAL, inverted, and steered to the proper output channel, while for D positive no pulse is transmitted.

The steering circuitry consists of the counting flip-flops A and B, connected to advance cyclically through four states, and the output gates NA 2 through NA5. The gates are connected to the counter such that a four position switch is formed, connecting the coincidence result on line 5 to a different output for each counter state.

The sequence of operation is as follows: A waveform at four times the modulation frequency is applied to the reference input, where it is shaped to trigger the pulser P1. The leading edge of the resulting phase triggers P2 and advances the counter A and B. The pulse from P1 is also inverted so that the trailing edge triggers P3, forming the coincidence pulse. This is conditionally transmitted through NA1 to the appropriate output. The pulse from P1 is approximately 3 microseconds long, hence the polarity determination is delayed by this amount with respect to the sampling and switching processes. This is to assure that all transients associated with sampling and switching have died out and no spurious outputs are obtained. The above sequence is repeated at the reference frequency (4 times the modulation frequency), with the counter advancing by

one for each repetition. Thus, the pulses appearing at the outputs 0_0 through 0_3 correspond to negative polarity coincidences at four equally spaced phase points of the modulation cycle.

For convenience, two subsidiary outputs are added. The output of the flip-flop B is a square wave at the modulation frequency. To avoid the necessity of synchronizing the reference oscillator with a separate modulation oscillator, this square wave is made available. In addition, another gate is added, NA6. This is switched in parallel with NA2 and connected directly to the inverted pulse from P3. This gives a pulse for each modulation cycle and is used as a clock for the automatic counting equipment.

Circuit Description

The PCD is constructed of solid state components. Pnp transistor-diode logic is used and the sampling and limiting circuits are solid state amplifiers.

The sample-and-hold circuit is shown in Fig. 2. The transistors Q_1, Q_2, and Q_3 comprise a 2 stage differential amplifier gated by Q_4. The gate input is normally at -12 volts which holds Q_4 at cutoff. The amplifier is gated on when the gate input is driven to ground potential. This is accomplished by a pulse of 1/2 microsecond duration. The transistors Q_6 and Q_7 form a cathode follower output. Q_6 is a field effect transistor which has a very high input impedance. The feedback to the differential input produces an overall gain of unity.

When the amplifier is gated on, the output is set equal to the input. In the process C_1 is charged to the output voltage. When the gating pulse disappears, the impedance at C_1 is very high due to Q_6 and

the back biased diodes D_1 and D_2. The charged capacitor thus holds the output voltage at the value set. The decay of the voltage on C_1 due to leakage was determined experimentally and found to be 1 volt per second, which is negligible for modulation frequencies about 100 Hz.

The linear amplifiers are Fairchild μ A702A monolythic operational amplifiers, connected as shown in fig. 3. α1 has a voltage gain of 50 and is externally frequency compensated to give amplification up to 100 kHz. α2 and α3 have diode feedback to give full open loop gain for small amplitude and clamp the output at twice the forward drop of the diode.

The details of the logic blocks are shown in fig. 4, 2N404 transistors are used except where higher switching speeds are needed as noted. Switching times are typically 0.2 microseconds. The voltages used as logic levels are -12 volts, designated as "0", and ground potential, designated as "1".

DC voltages required to operate the PCD are -12 volts at 150 ma, -12 volts at 200 ma, and -6 volts at 100 ma. The present model uses 2 Kepco model PAX 15-0.75 modular power supplies for -12 and -12 volts, and a separate regulator to provide -6 volts. Power input to the linear circuitry is filtered to prevent interaction with logic transients.

III. Data Accumulator

General Description

The use of long integration times requires very reliable methods for data acquisition. The equipment used to collect data from the PCD has a logical structure that enables the unit to perform serial-decimal addition and subtraction on the contents of each of three data registers, R_A, R_B, and R_C, a fourth register. Z, is used to hold the contents of the data registers

during shifting. The contents of the registers may be modified in a manner determined by "wired in" programs and by input data transmitted from the PCD in five channels. The accumulated information is stored in binary coded decimal form, each decimal digit being displayed in a group of four inductor lights. The device has two programs available. Depending upon the position of the program switch, either of the following sequences may be executed.

Program 1	Program 2
$R_A + 1 \rightarrow R_A$	$R_A + 1 \rightarrow R_A$
$R_B + 1 \rightarrow R_B$	$R_B + 1 \rightarrow R_B$
$R_A + 1 \rightarrow R_A$	$R_A - 1 \rightarrow R_A$
$R_B + 1 \rightarrow R_B$	$R_B - 1 \rightarrow R_B$
$R_C + 1 \rightarrow R_C$	$R_C + 1 \rightarrow R_C$

The execution of each of the five steps is enabled by the five lines from the PCD. Program 1 is used for calibration and program 2 performs the actual data accumulation corresponding to equation (6); namely, recording the difference counts of channels 0-2 and 1-3.

Figure 5 illustrates the organization of the device. The program sequencing unit (PSU) receives information from the PCD that determines the desired register modifications. The PSU also provides signals to the adder control and switch selection circuitry that initiate addition and control, which registers are being modified.

The adder control initiates the signals that transfer information between the data registers and the "A" registers and from the adder output to the A1 register.

The adder is a four bit binary, ripple carry, carry sensing type. The binary sums are converted to decimal in separate circuits. Adder inputs are always connected to the A1-A2 registers.

Figure 6 illustrates the connections between the registers and the adder. The contents of any of the three data registers may be transferred to the A1-A2 registers shifted right by one digit position. Data transfers from the "A" registers back to the data registers are performed without shifting. A transfer of data from a data register to the A1 register and back to the data register constitutes a shift of the data by one digit position. This process serves to sequentially connect each decimal digit, starting with the least significant, to the adder input. A total of eight shifts are required to perform an addition.

Control Sequencing

Control sequencing processes are frequently categorized as being either synchronous or asynchronous. The synchronous control performs operations at a fixed or some multiple of a fixed time interval. An asynchronous control attempts to initiate new operations immediately upon completion of the preceding one. This device employs an asynchronous control.

The program sequencing and storage unit, and the adder control, consist of cascaded logical circuits called sequencing blocks (SB). A logical diagram of a simple sequencing block is shown in fig. 7. Typically, the "advance out" signal of one SB is connected to the "advance in" terminal of another. All signals are a "one" when enabled, so that, if the flip-flop is the "zero" state, the "advance in" signal enables the advance circuit with no operation being performed. A "one" having been stored in the flip-flop

results in "advance in" actuating the "action request" line. "Action on" is a busy signal from the operation initiated by the "action request" signal. The "action request" signal remains a "one" until the flip-flop has been set to "zero." When the "action" signal returns to "zero" the advance circuit is enabled.

Designing a control using sequencing blocks is a systematic and straight forward procedure; furthermore, such a control is amenable to modification and lends itself well to diagnosis of malfunction and to electrical checking of the sequencing operation.

Figure 8 is a simplified logical diagram showing how sequencing blocks are employed in the program sequencer and the adder control. In the adder control, the flip-flops are always set to "one" before an addition since all steps are always required. When all SB's are known to produce "action" signals, it is possible to have an asynchronous control circuit with a minimum number of circuit delays required by the control. This is accomplished by allowing the "advance" signal from the SB requesting an action to propogate before the action is complete. The following operation is then inhibited by the busy signal from the preceding one at the latest possible logical level. This technique is employed in the adder control.

The flip-flops in the program sequencer are either set to a "one" or to a "zero" depending upon the outputs of the PCD. Each flip-flop corresponds to one of five register modifications that may be initiated whenever a clock signal appears. Whether the registers are altered or not depends upon data gathered by the PCD during the preceding clock interval.

Subtracting one from the contents of a register is implemented by tens complement addition.

When using program two, it must be determined whether the result held in a data register is in true or complement representation. This requires knowledge about the incoming data. For example, if the data registers are originally set to zero and the maximum number of forward counts is limited to 9,999,999 and the maximum number of backward counts to 10,000,000 then:

(a) The most significant digit of a number is always either zero or nine.

(b) If the most significant digit is a zero, net positive counts are indicated. If the most significant digit is a nine, the number of net negative counts is obtained by subtracting the register contents from 100,000,000.

There are two operations that may be initiated manually. They are:

$$R_c - R_A \rightarrow R_c$$

$$R_c - R_B \rightarrow R_c$$

By performing these operations with R_c initially equal to zero, the result is to complement the contents of R_A or R_B.

Summary

An improved PCD has been constructed. Improved stability and higher reliability are achieved through the use of solid state circuitry. The sensitivity of the device is increased by sampling four times per modulation cycle and by employing the same coincidence stage for all output channels. The high stability permits the use of integration times in excess of 10^6 sec., which is more than sufficient in most applications.

The data accumulator is also solid state for high reliability, featuring arithmetic units instead of straight counters, a direct display of the opposite phase channel differences, and automatic stop for any integration time. In addition, the complete system offers greater convenience because of the small physical size and low power consumption.

An example of the performance of the device is shown in fig. 9, which is a calibration of the PCD in conjunction with an X- band microwave receiver. This was obtained by switching the receiver input between two loads at the PCD modulation frequency. The two loads are; a matched load at room temperature produced by a standard noise source in conjunction with a precision attenuator. The ordinate is the signal-to-noise ratio at the input of the PCD and the abcissa is the temperature difference.

Reference

1. M. Raether and D. Bitzer, Rev. Sci. Instr. 35, 837, 1964.

Acknowledgement

We would like to thank Mr. J. Stifle for his technical assistance in the design of the PCD-circuitry.

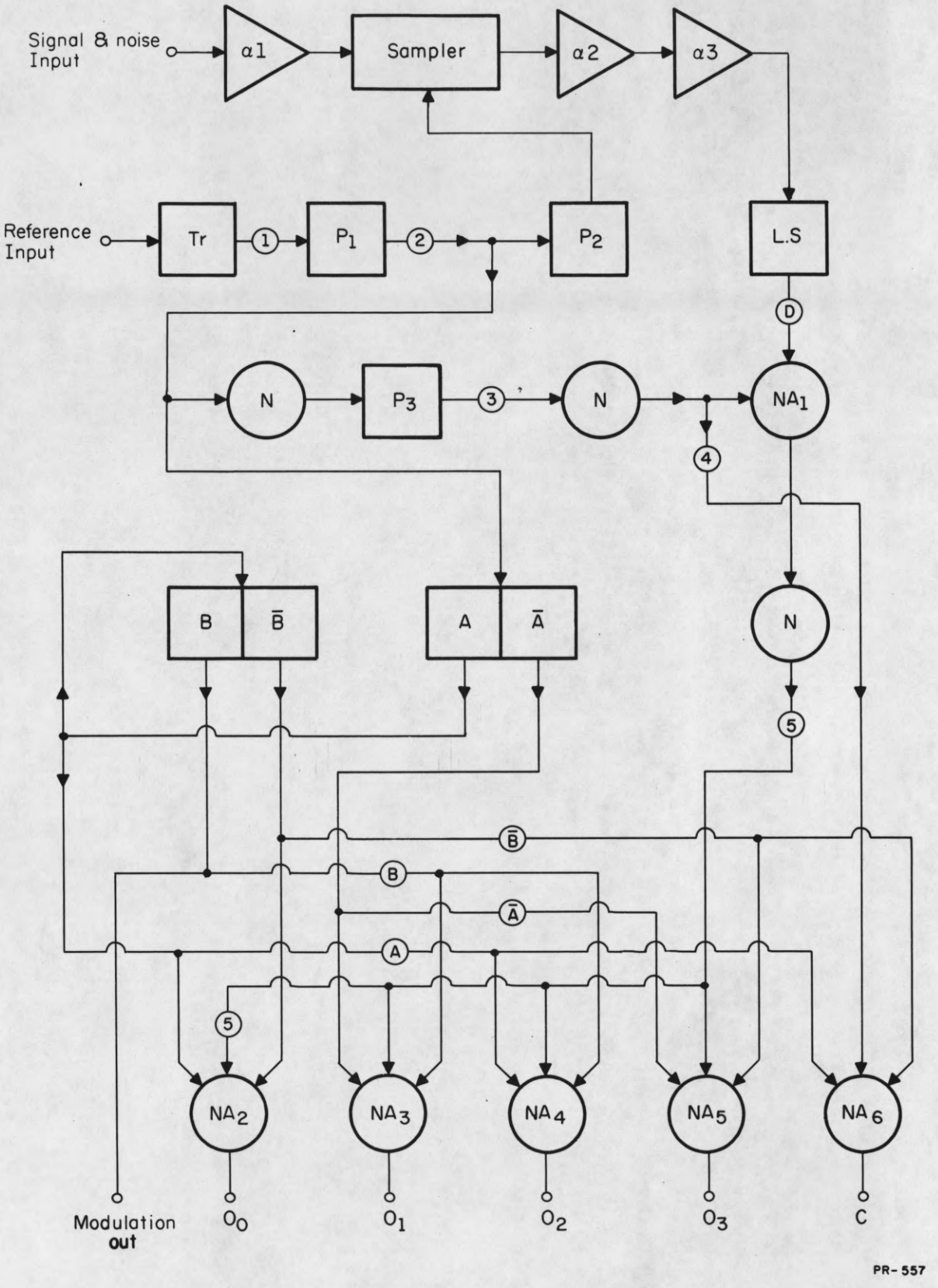

Figure 1. Block Diagram of the PCD.

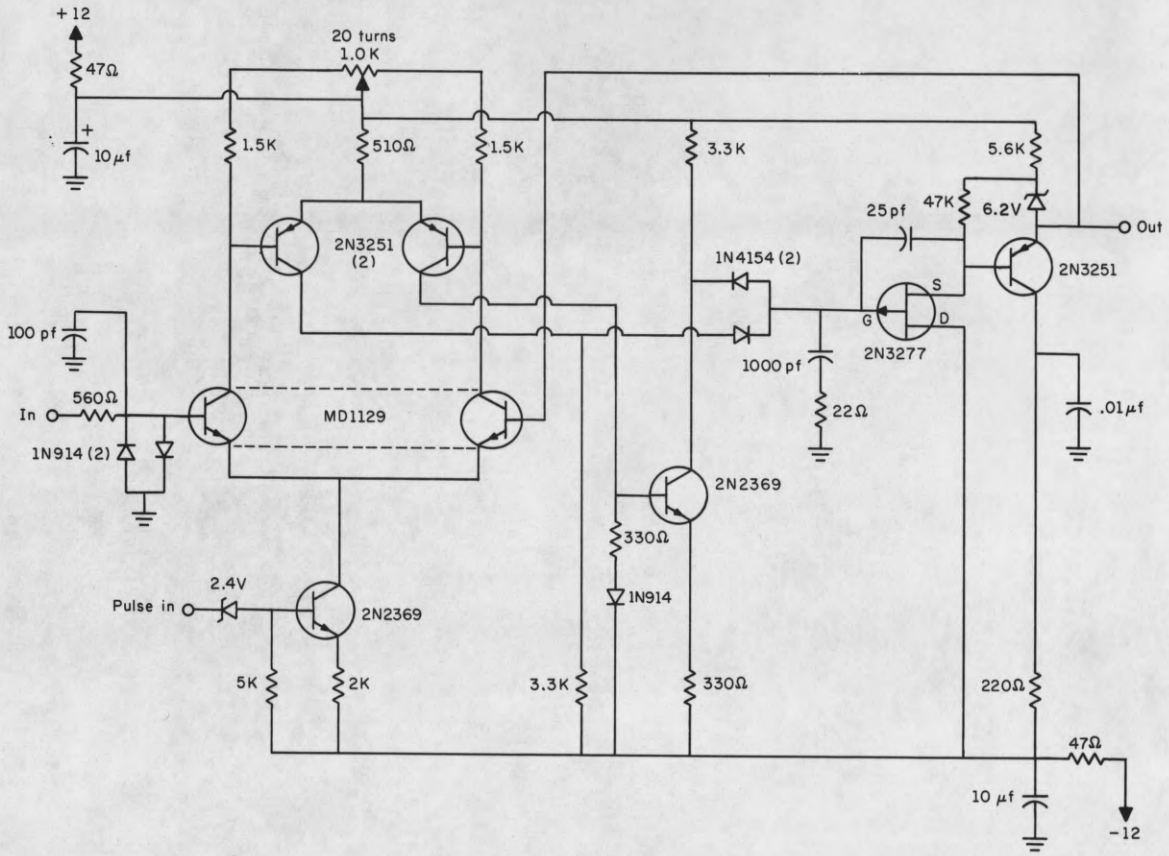

Figure 2. Diagram of the sample-and-hold circuit.

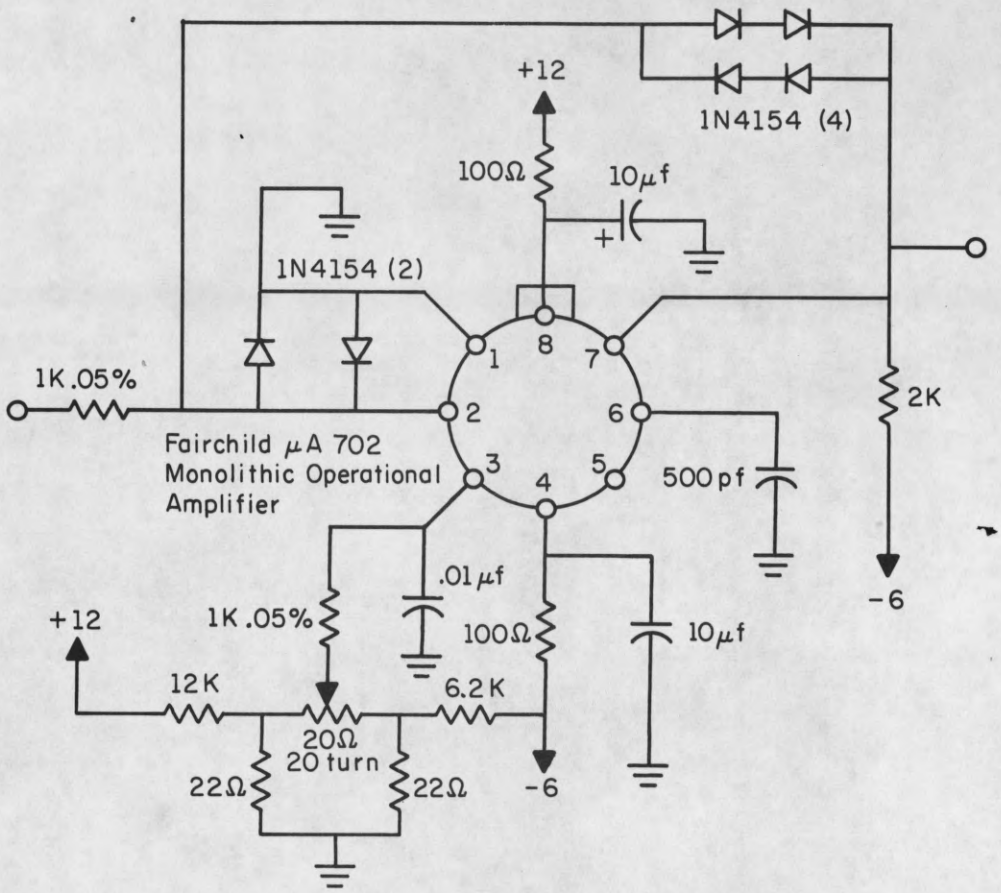

Figure 3. Circuit diagram of linear amplifier.

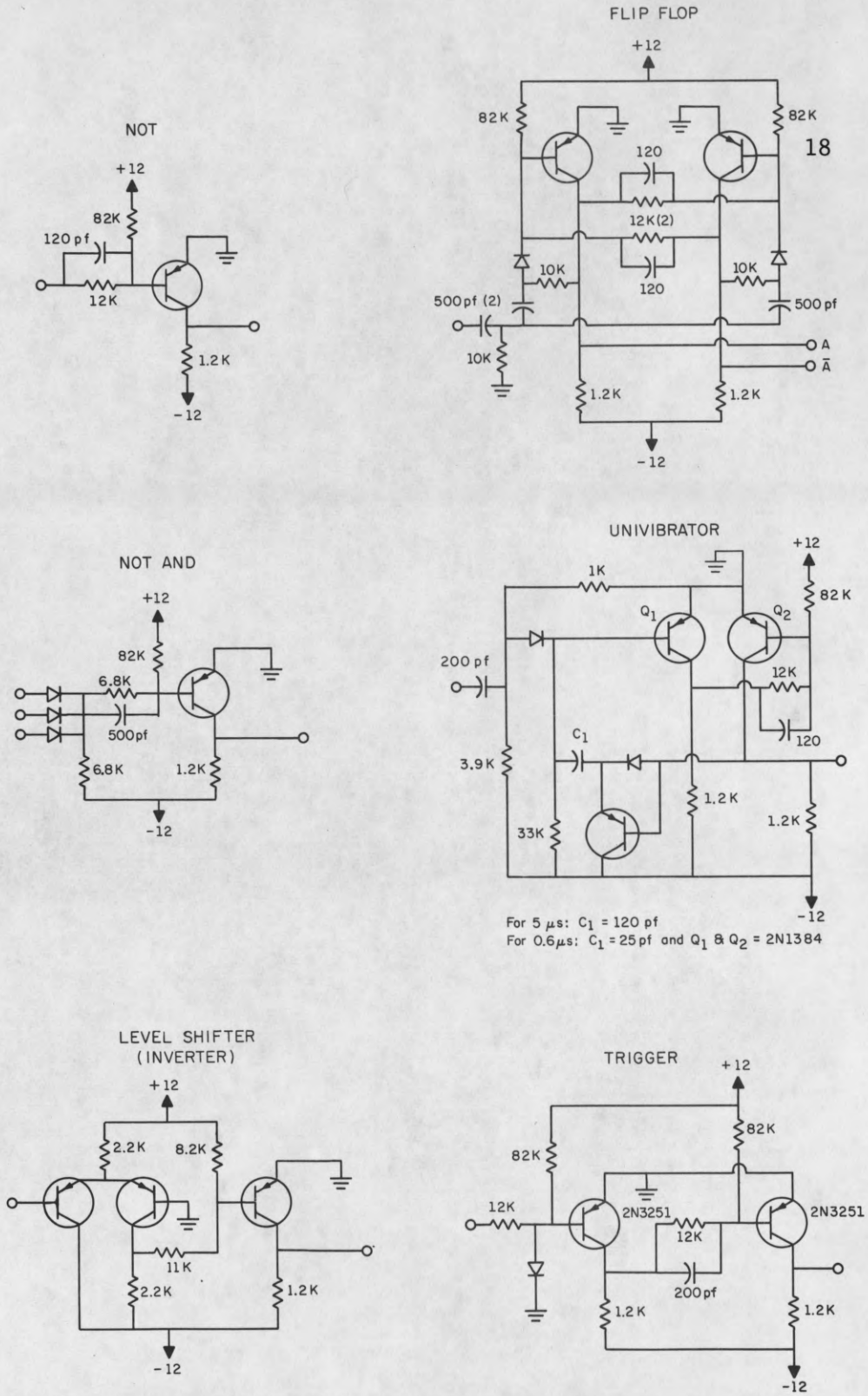

Figure 4. Circuit diagrams of the logic blocks.

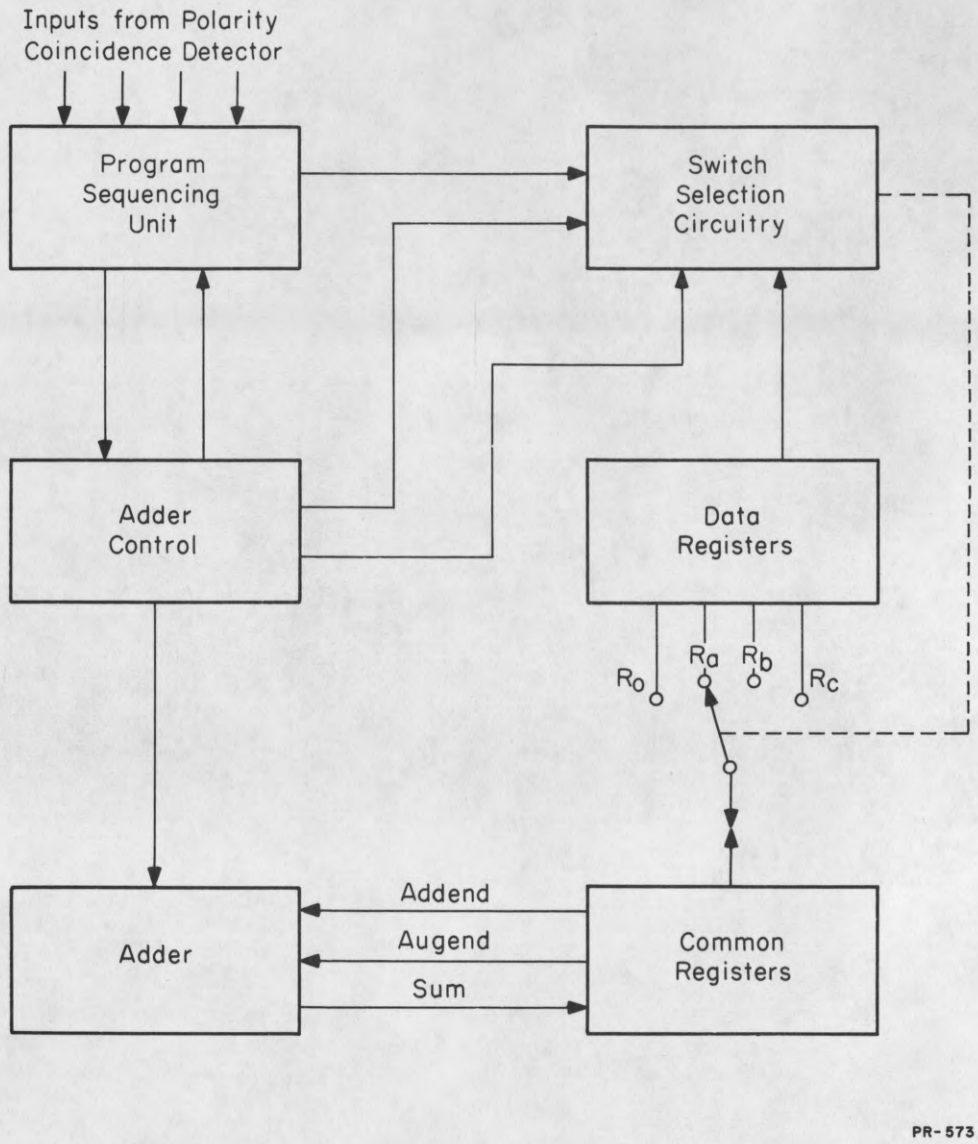

Figure 5. Block diagram of the data acquisition unit.

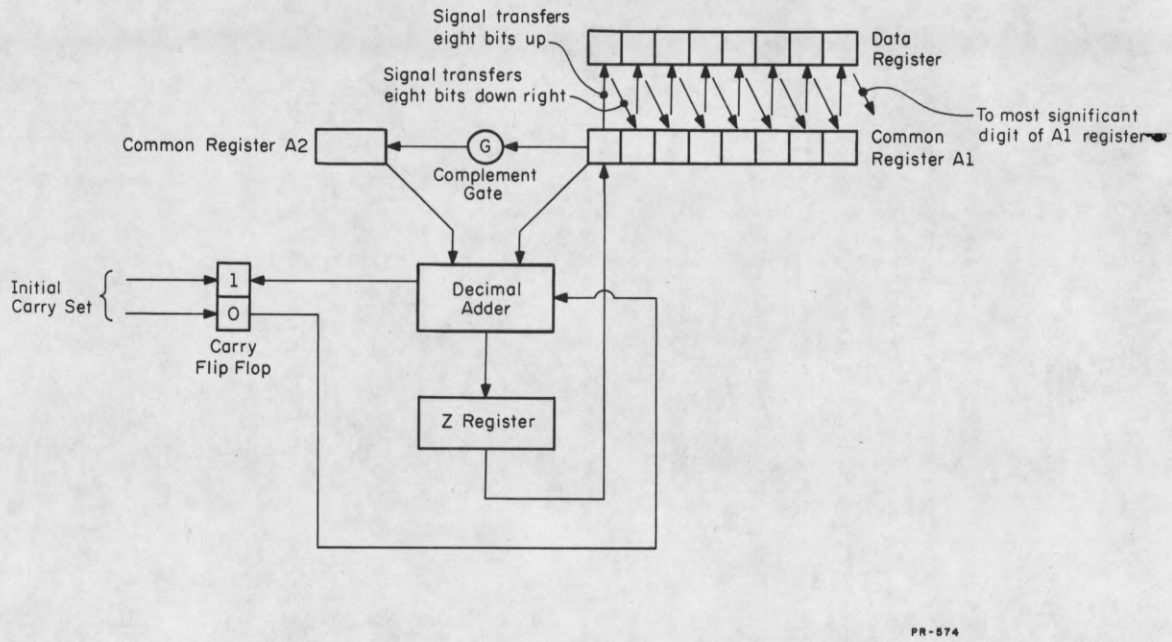

Figure 6. Interconnection between registers and adder.

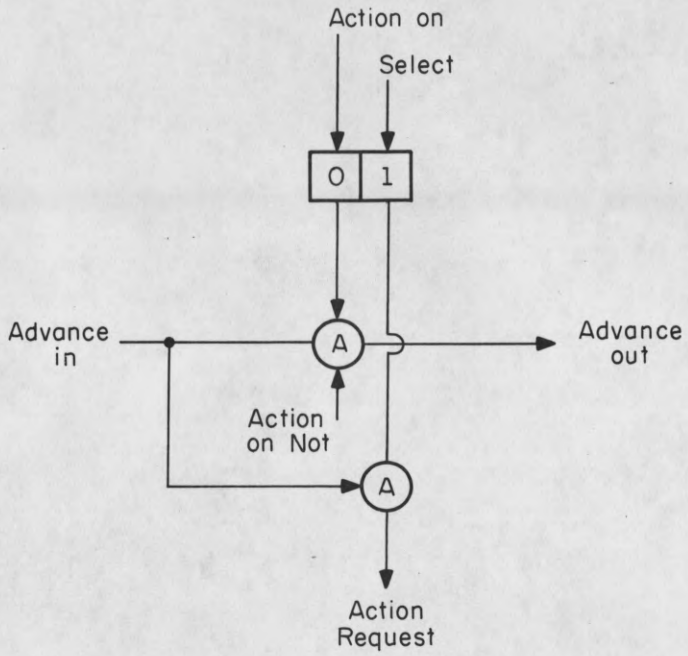

Figure 7. Block diagram of sequencing unit.

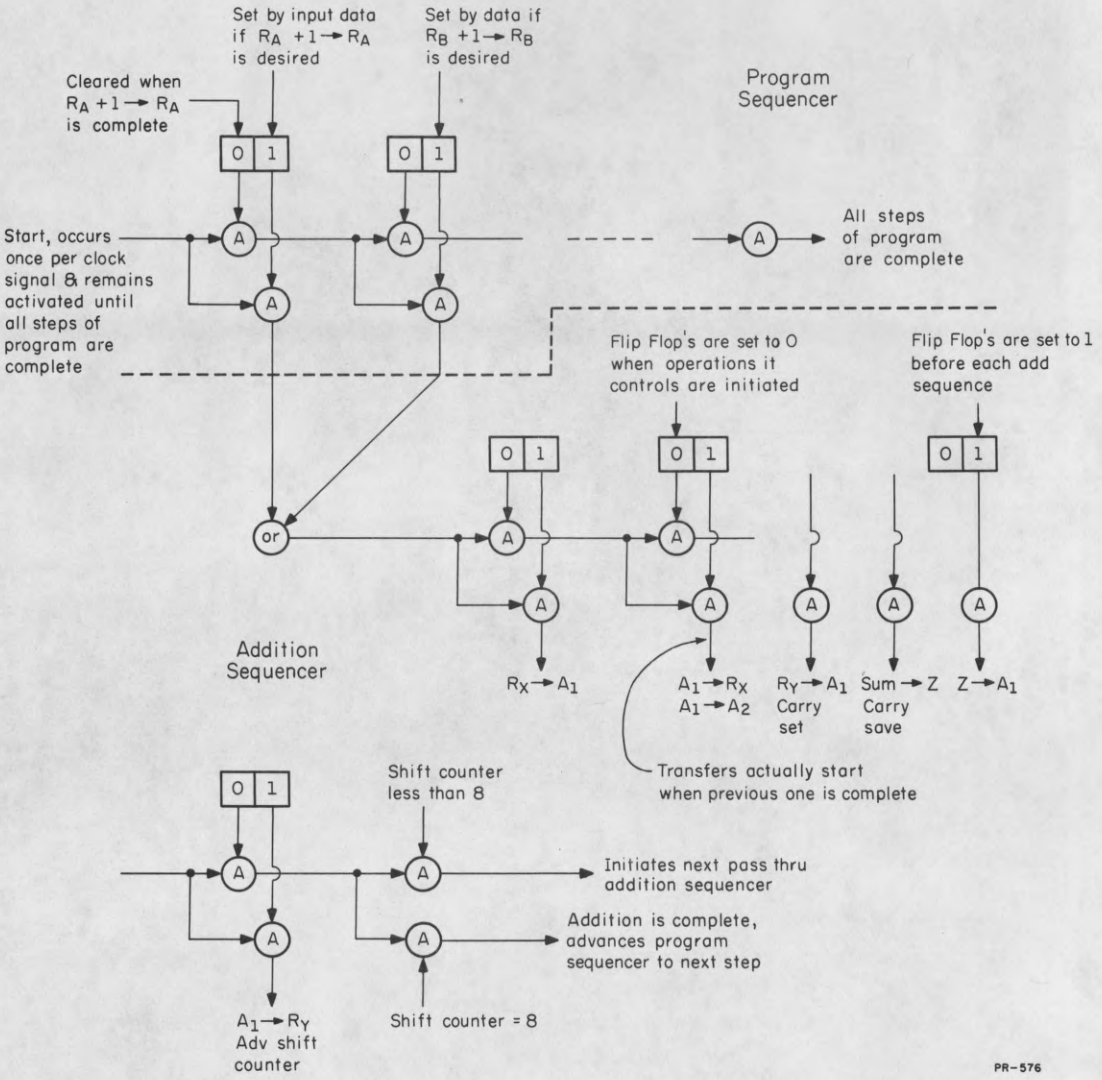

Figure 8. Incorporation of sequencing blocks in program sequencer and adder control.

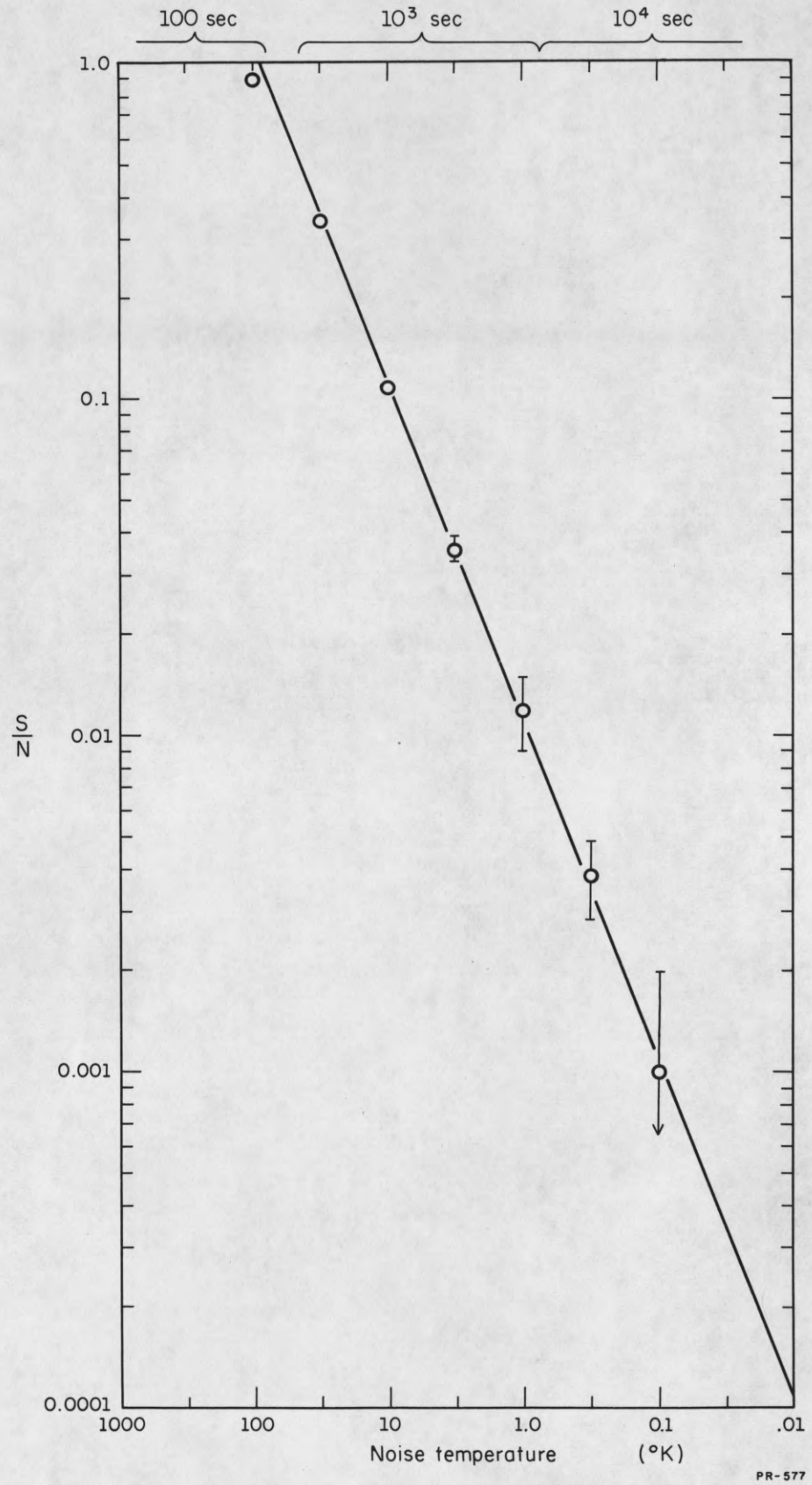

Figure 9. Performance of the PCD in conjunction with an X-band microwave receiver. The numbers at the top line give the integration times employed for the indicated accuracy.

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Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY *(Corporate author)*
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Urbana, Illinois 61801

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP

3. REPORT TITLE

AN IMPROVED POLARITY COINCIDENCE DETECTOR

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

5. AUTHOR(S) *(First name, middle initial, last name)*

W.E. Carr, M. Raether & R. Trogdon

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
September, 1967	23	1

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
DAAB07-67-C-0199	R-367
b. PROJECT NO.	
c.	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*
d.	

10. DISTRIBUTION STATEMENT

Distribution of this report is unlimited

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Joint Services Electronics Program thru U.S. Army Electronics Command Ft. Monmouth, New Jersey 07703

13. ABSTRACT

A Polarity Coincidence Detector has been constructed with increased sensitivity and sufficient threshold stability to allow integration times in excess of 10^6 sec. The system uses sampling at four phase locations, thereby increasing the signal count and shortening the integration time for a given accuracy by eliminating the necessity for measuring the noise separately. The modulation frequency can be varied between 50Hz and 50 kHz without adjusting the location of the sampling pulses. Solid state circuitry is used throughout the system. The straight counters are replaced by arithmetic units, resulting in greater dependability.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Synchronous Detector						
Polarity Coincidence detection						
Small signal-tonoise ratios						
Long integration times						